Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (canceled) A method for securing data of a data carrier comprising:

determining a current state of a memory, wherein the memory comprises a plurality of
    memory cells and wherein the current state of the memory is selected from the
    group consisting of an active state and a quiet state and wherein in the active state
    the data of the data carrier is accessible and wherein in the quiet state the data of the
    data carrier is inaccessible;

if the memory is in the active state, then determining a current state of a memory cell,
    wherein the current state of the memory cell is selected from the group consisting of
    a programmed state and an unprogrammed state; and

if the current state of the memory cell is the unprogrammed state, then selecting the
    memory cell and programming the selected memory cell to change the current state
    of the memory cell to the programmed state, wherein the memory cell assumes an
    irreversible memory state as a result of the programming and wherein the memory
    enters the quiet state.

2. (canceled) The method according to claim 1 further comprising, prior to determination
of the current state of the memory, verifying authorization to access the memory.

3. (canceled) The method according to claim 1, wherein determining a current state of a
memory comprises;

associating the active state with an even count of memory cells in the programmed state;

determining a count of memory cells in the programmed state;

if the count of memory cells in the programmed state is even, then determining the
    current state of the memory to be the active state; and

if the count of memory cells in the programmed state is odd, then determining the current
state of the memory to be the quiet state.

4. (canceled) The method according to claim 1, wherein determining a current state of a
memory comprises;
associating the active state with an odd count of memory cells in the programmed state;
determining a count of memory cells in the programmed state;
if the count of memory cells in the programmed state is odd, then determining the current
state of the memory to be the active state; and
if the count of memory cells in the programmed state is even, then determining the
current state of the memory to be the quiet state.

5. (currently amended) An integrated circuit for securing data stored in a data carrier
comprising:
a memory comprising a plurality of memory cells, wherein the memory comprises a
plurality of memory cells;
a first logic circuit configured for determining a current state of the memory, wherein the
current state of the memory is selected from the group consisting of an active state
and a quiet state and wherein in the active state the data of the carrier is accessible
and wherein in the quiet state the data of the carrier is inaccessible;
a feed-logic circuit, wherein the feed-logic circuit is configured for:
receiving state information indicative of a current state of a memory cell, wherein
the current state of the memory cell is selected from the group consisting of
a programmed state and an unprogrammed state; and
if the current state of the memory is the active state and if the current state of the
memory cell is the unprogrammed state, then selecting the memory cell; and
issuing a programming command to a the programming unit to program the
selected memory cell to change the state of the memory cell to the
programmed state, wherein the memory cell assumes an irreversible
memory state as a result of the programming and wherein the memory
enters the quiet state;

means for returning the memory back to the active state and then resetting the memory to the quiet state by changing the state of a next memory cell of the plurality of memory cells to the programmed state, wherein said next memory cell assumes an irreversible memory state as a result of the programming.

6. (previously presented) The integrated circuit according to claim 5 further comprising:

a counter; and

a sequencing circuit, wherein the sequencing circuit is configured for:

      providing a clock signal to a clock input of the integrated circuit via the counter;

      receiving a serial output from the integrated circuit indicative of the state of each of the plurality of memory cells; and

      issuing a stop count signal to the counter when a first memory cell in the unprogrammed state is detected, and

wherein the counter is configured to count the clock signals to produce a count indicative of the location of the first memory cell in the unprogrammed state.

7. (canceled)

8. (previously presented) The integrated circuit according to claim 5 further comprising a verification circuit, wherein the verification circuit is configured for, prior to determination of the current state of the memory, verifying authorization to access the memory.

9. (previously presented) An integrated circuit according to claim 5, wherein the data stored in the data carrier is selected from the group consisting of preset data and data entered via an input device.

10. (previously presented) A data carrier comprising an integrated circuit according to claim 5.

11. (original) A data carrier according to claim 10, wherein the data carrier is designed for contactless communication with a communication station.

12. (previously presented) A data carrier according to claim 10, wherein the data carrier is in the form of a tag or label.

13. (previously presented) The integrated circuit of claim 5, wherein the active state is associated with an even count of memory cells in the programmed state and wherein the first logic circuit is configured for:

determining a count of memory cells in the programmed state;

if the count of memory cells in the programmed state is even, then determining the
   current state of the memory to be the active state; and

if the count of memory cells in the programmed state is odd, then determining the current
   state of the memory to be the quiet state.

14. (previously presented) The integrated circuit of claim 5, wherein the active state is associated with an odd count of memory cells in the programmed state and wherein the first logic circuit is configured for:

determining a count of memory cells in the programmed state;

if the count of memory cells in the programmed state is odd, then determining the current
   state of the memory to be the active state; and

if the count of memory cells in the programmed state is even, then determining the
   current state of the memory to be the quiet state.

15. (new) An integrated circuit for securing data stored in a data carrier comprising:

a memory comprising a plurality of memory cells;

a first logic circuit configured for determining a current state of the memory, wherein the
   current state of the memory is selected from the group consisting of an active state
   and a quiet state and wherein in the active state the data of the carrier is accessible
   and wherein in the quiet state the data of the carrier is inaccessible;

a feed-logic circuit, wherein the feed-logic circuit is configured for:

receiving state information indicative of a current state of a memory cell, wherein
the current state of the memory cell is selected from the group consisting of
a programmed state and an unprogrammed state; and

if the current state of the memory is the active state and if the current state of the
memory cell is the unprogrammed state, then selecting the memory cell; and

issuing a programming command to a programming unit to program the selected
memory cell to change the state of the memory cell to the programmed state,
wherein the memory cell assumes an irreversible memory state as a result of
the programming and wherein the memory enters the quiet state;

wherein the active state is associated with an even count of memory cells in the

programmed state and wherein the first logic circuit is configured for:

determining a count of memory cells in the programmed state;

if the count of memory cells in the programmed state is even, then determining the
current state of the memory to be the active state; and

if the count of memory cells in the programmed state is odd, then determining the current
state of the memory to be the quiet state.

16. (new) An integrated circuit for securing data stored in a data carrier comprising:

a memory comprising a plurality of memory cells;

a first logic circuit configured for determining a current state of the memory, wherein the
current state of the memory is selected from the group consisting of an active state
and a quiet state and wherein in the active state the data of the carrier is accessible
and wherein in the quiet state the data of the carrier is inaccessible;

a feed-logic circuit, wherein the feed-logic circuit is configured for:

receiving state information indicative of a current state of a memory cell, wherein
the current state of the memory cell is selected from the group consisting of
a programmed state and an unprogrammed state; and

if the current state of the memory is the active state and if the current state of the
memory cell is the unprogrammed state, then selecting the memory cell; and

issuing a programming command to a programming unit to program the selected
memory cell to change the state of the memory cell to the programmed state,

wherein the memory cell assumes an irreversible memory state as a result of the programming and wherein the memory enters the quiet state;

wherein the active state is associated with an odd count of memory cells in the programmed state and wherein the first logic circuit is configured for:

determining a count of memory cells in the programmed state;

if the count of memory cells in the programmed state is odd, then determining the current state of the memory to be the active state; and

if the count of memory cells in the programmed state is even, then determining the current state of the memory to be the quiet state.